REMARKS

At the time the Official Action was mailed, claims 1-49 were pending. Claims 1-8, 13-30, 35-41 and 43-49 stand rejected. The Examiner objected to claims 9-12, 31-34 and 42 as being dependent on rejected base claims. Claims 1, 5, 9, 27, 31, 39, 42 and 45-47 have been amended, and claims 4, 30 and 44 have been cancelled. New claim 50 has been added. Reconsideration of the application in view of the remarks set forth below is respectfully requested.

Allowable Subject Matter

Applicant thanks the Examiner for the indication of allowable subject matter. Based on the Examiner's indication of allowable subject matter, claims 9, 31 and 42 have been amended to place the claims in independent form. Applicant respectfully submits that claims 9-12, 31-34 and 42 are presently in condition for allowance.

Rejections Under 35 U.S.C. § 102

The Examiner rejected claims 1-49 under 35 U.S.C. § 102(b) as being anticipated by Garbus et al. (U.S. Pat. No. 5,884,027), hereinafter "Garbus." In the present Final Office Action, mailed on June 1, 2004, the Examiner maintained the same rejections as set forth in the prior Office Action mailed on December 19, 2004. In the Final Office Action the Examiner also addressed Applicant's prior arguments and summarized his points of contention with Applicant's arguments as follows:

> 1) Garbus explicitly teaches primary and secondary buses [fig. 2] which are PCI bus and VGA bus [col. 6, lines 17-25] via I/O communication. Thus, Garbus teaches "an I/O bus selectively comprising one of a first bus type and a second bus type," as recited in the present claims.
>
> 2) Garbus explicitly teaches a "Master/Slave" networking communication environment [col. 7, lines 36-52]. Garbus inherently demonstrates fail-over, redundancy or backup functionality or

> capability within the networking buses error detection and failure recovery. Thus, Garbus teaches performing a transaction over a portion of an I/O bus if an error is detected on an alternate portion of the I/O bus. More specifically, Garbus teaches a device interface connectable to an I/O bus having a first bus portion and a second bus portion, wherein "if a first error is detected on the first bus portion, then the transaction is performed over the second bus portion," and wherein "if a second error is detected on the second bus portion, then the transaction is performed over the first bus portion."

Applicant respectfully traverses these rejections. Anticipation under Section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under Section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under Section 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Thus, if the claims recite even one element not found in the cited reference, the reference does not anticipate the claimed invention.

Because the Examiner rejected independent claims 27 and 39 under the same rationale as applied to claim 1, the present response will specifically address those features explicitly recited in claim 1. However, based on the Examiner's rejection and the presently recited subject matter, it should be understood that the present response is directed to each of independent claims 1, 27 and 39. Further, portions of the present response also pertain to the elements recited in new claim 50.

Applicant respectfully traverses the Examiner's rejection of claim 1 for at least three reasons. First, Garbus does not disclose "a core logic chipset comprising a bridge interface configurable to implement either one of an accelerated graphics bus bridge and a peripheral

component interconnect bridge." Second, Garbus does not disclose "an I/O bus selectively comprising one of a first type bus and a second type bus, wherein the first type bus comprises an accelerated graphics port bus, and the second type bus comprises a peripheral component interconnect bus." Third, the Garbus reference does not disclose performing a transaction over a portion of an I/O bus if an error is detected on an alternate portion of the I/O bus. More specifically, Garbus does not disclose a device interface connectable to an I/O bus having a first bus portion and a second bus portion, wherein "if a first error is detected on the first bus portion, then the transaction is performed over the second bus portion," and wherein "if a second error is detected on the second bus portion, then the transaction is performed over the first bus portion."

With regard to the first and second points, claim 1 recites "a core logic chipset comprising a bridge interface configurable to implement either one of an accelerated graphics bus bridge and a peripheral component interconnect bridge." Claim 1 further recites "an I/O bus selectively comprising one of a first type bus and a second type bus, wherein the first type bus comprises an accelerated graphics port bus, and the second type bus comprises a peripheral component interconnect bus." As discussed in the background of the present specification, it would be desirable to provide a computer system having a core logic chipset *configurable* for either an accelerated graphics port (AGP) bus or a peripheral component interconnect (PCI) bus without requiring different logic and interface circuits for each *type* of bus. Specification, page 8, lines 15-17. The present invention advantageously provides a system configured for selecting an I/O bus type in the core logic chipset. Selection of the type of bus bridge (i.e., PCI or AGP) in the core logic chipset may be made by a hardware signal input, by software during computer system configuration or by a power on self test ("POST"). Specification, page 11, line 20 - page 12, line 1. Thus, as clearly set forth in the claims, the presently recited system includes a core logic chipset comprising a bridge interface *configurable to implement*

a selected one of an AGP bridge or a PCI bridge. Further, the presently recited system includes an I/O bus selectively comprising a first bus type (AGP bus) and a second bus type (PCI).

In contrast, Garbus discloses a PCI-to-PCI bridge 31, primary PCI bus 17 and a secondary PCI bus 19. The Examiner correlated the presently recited core logic chipset with the PCI-to-PCI bridge 31 disclosed in Garbus and correlated first bus portion and second bus portion of the I/O bus with the PCI buses 17 and 19 disclosed in Garbus. However, the Examiner failed to cite any portion of Garbus that indicates that the I/O bus is selective between a first type bus and a second type bus, wherein the first type bus is an AGP bus and the second type bus is a PCI bus, as also recited in claim 1. Indeed, if the Examiner is asserting that the primary PCI bus 17 of Garbus is comparable to the first portion of the I/O bus recited in claim 1 and that the secondary PCI bus 19 of Garbus is comparable to the second portion of the I/O bus recited in claim 1, the rejection is improper since it is clear that each of the buses 17 and 19 has the same bus type. Accordingly the I/O bus disclosed in Garbus can hardly be characterized as "s*electively* comprising one of a first type bus and a second type bus," (emphasis added), much less that the I/O bus selectively comprises one of an AGP bus and a PCI bus, as further recited in claim 1. That is to say that each of the buses 17 and 19 disclosed in Garbus can be one and only one type of bus: a PCI bus.

Similarly, the PCI-to-PCI bridge 31 disclosed in Garbus does not include a configurable bridge interface, but is simply implemented as a PCI bridge compatible with PCI devices and PCI buses. Clearly, the PCI-to-PCI bridge interface disclosed in Garbus *cannot* be used in conjunction with an AGP bridge. Accordingly, the PCI-to-PCI bridge 31 cannot possibly be configured to implement either an accelerated graphics bus bridge or an peripheral component interconnect bridge.

In fact, the Garbus reference fails to disclose an AGP bus, an AGP bridge or an AGP bridge interface, at all. In the Final Office Action, the Examiner stated that "Garbus explicitly teaches primary and secondary buses [fig. 2] which are PCI bus and VGA bus [col. 6, lines 17-25] via I/O communication." Applicant respectfully submits that the secondary bus 19 disclose in the Garbus reference is simply a PCI bus *compatible* with a video graphics array (VGA). Further, Applicants respectfully submit that the term "VGA bus" is not analogous to the term "AGP bus." The acronyms "PCI" and "AGP" refer to bus standards or interface specifications developed by Intel Corporation, while the acronym "VGA" refers to a graphics standards developed by IBM. As discussed briefly below, an accelerated graphics port (AGP) is not analogous to a video graphics array (VGA).

Generally, a Peripheral Component Interconnect (PCI) is a 64-bit bus, though it is usually implemented as a 32-bit bus. It can run at clock speeds of 33 or 66 MHz. At 32 bits and 33 MHz, it yields a throughput rate of 133 MBps. *See e.g.*, http://www.webopedia.com/TERM/P/PCI.html. Accelerated Graphics Port (AGP) is based on PCI, but is designed especially for the throughput demands of 3-D graphics. Rather than using the PCI bus for graphics data, AGP introduces a dedicated point-to-point channel so that the graphics controller can directly access main memory. The AGP channel is 32 bits wide and runs at 66 MHz. This translates into a total bandwidth of 266 MBps, as opposed to the PCI bandwidth of 133 MBps. AGP also supports two optional faster modes, with throughputs of 533 MBps and 1.07 GBps. In addition, AGP allows 3-D textures to be stored in main memory rather than video memory. *See e.g.*, http://www.webopedia.com/TERM/A/AGP.html. In summary and as appreciated by those skilled in the art, PCI and AGP refer to bus or interface standards.

In stark contrast, "VGA" refers to graphics standards or a graphics display system for personal computers. VGA has become one of the de facto standards for PCs. In text mode, VGA systems provide a resolution of 720 by 400 pixels. In graphics mode, the resolution is either 640 by 480 (with 16 colors) or 320 by 200 (with 256 colors). The total palette of colors is 262,144. Unlike earlier graphics standards, VGA uses analog signals rather than digital signals. *See e.g.*, http://www.webopedia.com/TERM/V/VGA.html. In summary and as appreciated by those skilled in the art, VGA refer to graphics standards.

In light of the aforementioned discussion, Applicants respectfully submit that while the Examiner correctly noted that the Garbus reference discloses that the secondary PCI bus 19 may be compatible with a VGA system, this point is irrelevant in the context of the presently recited subject matter. VGA compatibility cannot be properly correlated with an AGP bus.

Accordingly, Applicant respectfully submits that Garbus does not disclose "a core logic chipset comprising a bridge interface configurable to implement either one of an accelerated graphics bus bridge and a peripheral component interconnect bridge." Applicants further submit that Garbus does not disclose "an I/O bus selectively comprising one of a first type bus and a second type bus, wherein the first type bus comprises an accelerated graphics port bus, and the second type bus comprises a peripheral component interconnect bus." For these reasons alone, the Garbus reference cannot possibly anticipate the present claims.

With regard to the third point, claim 1 recites a device interface connectable to an I/O bus having a first bus portion and a second bus portion, wherein "if a first error is detected on the first bus portion, then the transaction is performed over the second bus portion," and wherein "if a second error is detected on the second bus portion, then the transaction is

performed over the first bus portion." As disclosed in the background of the present specification, it would be desirable to provide a system for improving fault tolerance on an I/O bus when either of the upper (first) or lower (second) 32-bit data-width portions of a 64-bit data-width bus may have an operating fault. Specification, page 10, lines 19-22. In accordance with embodiments of the present invention, these problems are overcome by providing a fault tolerant 64-bit data-width PCI/PCI-X/AGP bus system which may recover from faults occurring on either the upper or lower 32-bit portions of a 64-bit data-width bus. Specification, page 11, lines 18-22. Thus, in accordance with one embodiment, the present invention provides a computer system having a fault tolerant 64-bit data-width PCI, PCI-X or AGP bus system that may recover from any fault occurring on either the upper or lower portions of the 64-bit data-width bus. Specification, page 19, lines 20-23. As recited in claim 1, if an error is detected on the first (e.g., upper) bus portion, then the transaction is performed over the second (e.g., lower) bus portion and vice versa.

With regard to these features of the device interface of claim 1, the Examiner cited col. 7, lines 36-52 and tables 4b and 4c of Garbus. Further, the Examiner asserted that "Master/Slave" networking communication environment disclosed in Garbus indicates that if an error is detected on a first bus portion, the transaction is performed over the second bus portion. Applicant respectfully submits that Garbus does not disclose or teach a system having these characteristics. The primary and secondary PCI bus are each coupled to different PCI devices. Accordingly, errors occurring on the primary PCI bus may not be passable to the secondary PCI bus. Further, Garbus does not discuss performing transactions over a particular one of the buses if an error is detected on the other bus. Accordingly, Applicant asserts that Garbus does not disclose a device interface connectable to an I/O bus having a first bus portion and a second bus portion, wherein "if a first error is detected on the first bus portion, then the transaction is performed over the second bus portion," or wherein

"if a second error is detected on the second bus portion, then the transaction is performed over the first bus portion." For this additional reason, Applicant respectfully submits that Garbus cannot possibly anticipate the present claims.

For at least these reasons, Applicant respectfully submits that Garbus does not disclose each of the features recited in the present claims, and therefore, cannot possible anticipate the presently recited subject matter. Accordingly, Applicant respectfully requests withdrawal of the Examiner's rejection under 35 U.S.C. § 102 and allowance of claims 1-3, 5-29, 31-43 and 45-49.

Conclusion

In view of the remarks and amendments set forth above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1-3, 5-29, 31-43 and 45-49. Applicant also requests consideration and allowance of new claim 50. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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